

Substitute for Form 1449/PTO				Complete if Known		
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				Application Number	09/954,777	
				Filing Date	September 17, 2001	
				First Named Inventor:	Mark Greenberg	
				Art Unit	2631	
				Examiner Name	Not Yet Assigned	
Sheet	1	of	2	Attorney Docket Number	004259.P034	
<b>U.S. PATENT DOCUMENTS</b>						
Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)				
JAM		US-	4,015,238	3/29/1977	Robert Curtis Davis	
		US-	5,027,374	6/25/1991	Mark W. Rossman	
		US-	5,291,499 A	3/1/1994	Behrens et al.	
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FOREIGN PATENT DOCUMENTS								
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		Country Code <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
JAM		WO	00/74264	A1	12/7/2000	Martone, Massimiliano		
JAM		WO	01/59937	A2	8/16/2001	Qualcomm Inc.		

Examiner Signature	Jarol M... [Signature]	Date Considered	2/3/05
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Sheet	2	of	2	Attorney Docket Number	004259.P034
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<b>NON PATENT LITERATURE DOCUMENTS</b>					
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T <sup>2</sup>
JM		JAMES TSUI, "Frequency Channelization, Digital Techniques for Wideband Receivers," Second Edition, Pages 363-396, 2001 Artech House, Inc., Norwood, MA			
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		E. VERRIEST, ISEN, "Implementing an Adaptive Noise Canceling System to Enhance Sonar Receiver Performance Using the TMS320C31 DSP," ESIEE, Paris, September 1996, Texas Instruments, Pages 1-24.			
		G.A. SHAW, R.A. FORD, J.C. ANDERSON, B.W. ZUERDNORFER, A.H. ANDERSON, "RASSP Benchmark 2 Technical Description," Massachusetts Institute Of Technology Lincoln Library, 153 pages total.			
		BREE, ET AL., "A Bit-Serial Architecture For A VLSI Viterbi Processor", Communications Systems Research Group, University of Saskatchewan, Saskatoon, IEEE, WESCANEX '88, 1988, pages 72-77.			
		BIVER, ET AL., "Architectural Design and Realization Of A Single-Chip Viterbi Decoder", Elsevier Science Publishers B.V., INTEGRATION, The VLSI Journal 8 (1989), October, No. 1, Amsterdam, NL, Pages 3-16.			
		BREE, ET AL., "A Modular Bit-Serial Architecture For Large Constraint-Length Viterbi Decoding", Communications Systems Research Group, University of Saskatchewan, Saskatoon, Canada, IEEE International Conference on Communications", 1990, pages 1501-1506.			
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		MARIE-LAURE BOUCHERET, IVAR MORTENSEN and HENRI FAVARO, "Fast Convolution Filter Banks For Satellite Payloads with On-Board Processing," IEEE Journal On Selected Areas In Communications, Vol. 17, No. 2, February 1999			
		W.H. YIM and F.P. COAKLEY, "On-Board Processing For KA-Band Applications", University of Surrey, UK, Publication Date, February 11, 1993., XP 000458011, pp. 225-229.			
		HASHIDA MITSUYOSHI, "Hierarchical Network Management System and Control Method for Network Management Information," Patent Abstracts of Japan, Publication No. 07226777			

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PTO/SB/08A (10-01)

Approved for use through 10/31/2002. OMB 0651-0031

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Substitute for form 1449A/PTO

## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	1	of	2
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First Named Inventor	Mark Greenberg
Art Unit	2631
Examiner Name	Unassigned
Attorney Docket Number	4259P034

## U.S. PATENT DOCUMENTS

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## FOREIGN PATENT DOCUMENTS

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Sheet 2 of 2

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Examiner Name	Unassigned
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## OTHER ART - NON PATENT LITERATURE DOCUMENTS

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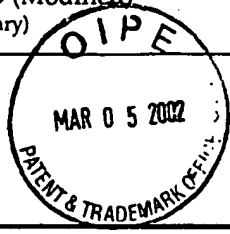
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 04259.P034	Application Number: 09/954,777
	First Named Inventor: Mark Greenberg, et al.	
	Filing Date: September 17, 2001	



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		Number	Kind Code <sup>3</sup> (If known)			
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		6,141,391		Morelos-Zaragoza, et al.	10/31/2000	
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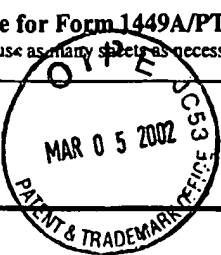
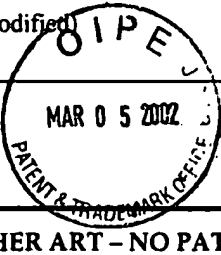
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JGM		JOHN G. PROAKIS, Block and Convolutional Channel Codes, Digital Communications, Fourth Edition, Pages 416 - 547, McGraw-Hill Series in Electrical and Computer Engineering, New York, NY.	
		"www.inventra.com/inventra/softcore/workshop/MultiRaFiltDes95/" MENTOR GRAPHICS, Hardware Design of Decimators/Interpolators, Pages 1-38.	
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